Imperial College
London

Lecture 4

Understanding op-amp models

Prof Peter YK Cheung
Imperial College London

URL: www.ee.ic.ac.uk/pcheung/teaching/EE2_CAS/
E-mail: p.cheung@imperial.ac.uk

In this week's lecture, you will learn how Spice model for MCP6001 is developed based on the datasheet information about the op-amp. The learning outcome is that you will be able to develop Spice models for other type of devices.

What is SPICE Simulator?

- Simulation Program with Integrated Circuit Emphasis
  - Developed by Larry Nagel at Berkeley in 1970's (under Prof Don Pederson).
  - Many commercial and freeware versions available.
  - Most significant CAD tool that drove the advancements in microelectronics.
- Linear Technology SPICE (LTspice)
  - Developed by Mike Engelhardt in early 2000s when he worked for Linear Technology (later bought by Analog Devices).
  - Added schematic capture and results plotting.
  - Engelhardt now has his own company marketing Qspice – not free.
- Input to SPICE is a SPICE netlist – multiple lines of text that describe:
  - Components and voltage/current sources in a circuit.
  - How the components and sources are connected to each other.
  - Model of components.
  - Type of analysis to be performed by the simulator

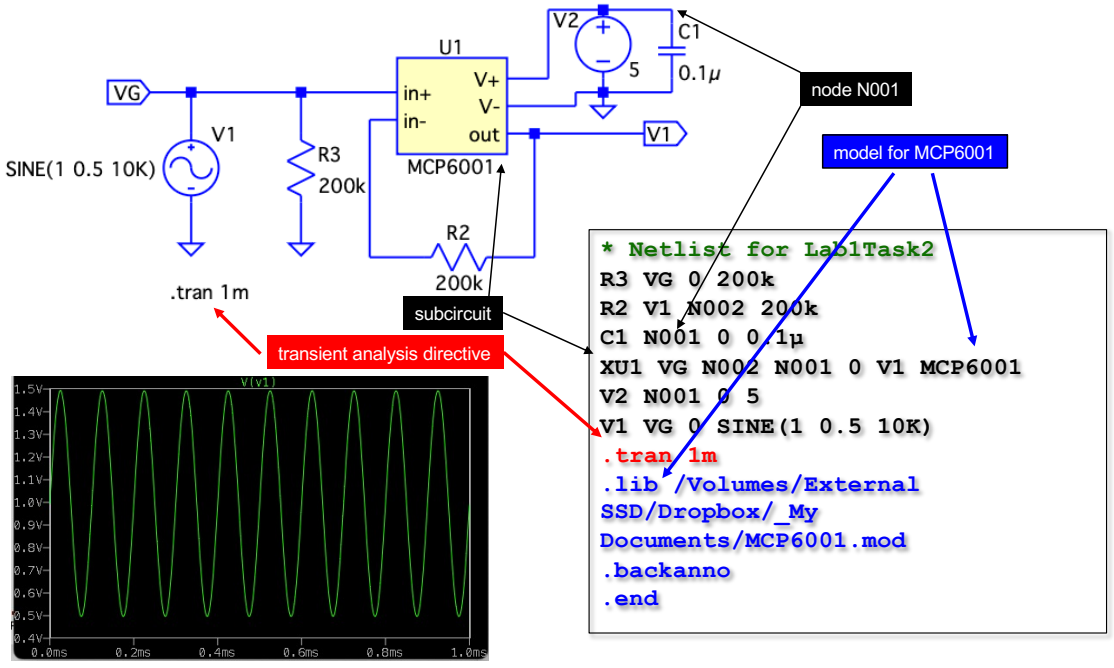
SPICE is a circuit level simulator developed in the 70's by a researcher, Larry Nagel, in Professor Don Pederson's research group. This simulator was open-sourced and free to use, and quickly became the de facto standard circuit level simulators for analogue and digital integrated circuits designed since.

LTSpice, which you used in Year 1 and in this modules lab experiments was based on the original SPICE program, but improved in several ways. The most significant improvement is the addition of schematic capture and waveform display.

The input to the original SPICE program was a text file that describes the circuits and the type of analysis to be performed by the simulator program. This file is called the **Spice netlist**.

LTSpice also generates the netlist which you can display by RIGHT-CLICK on th schematic and select **View > SPICE** netlist.

Example of a Spice netlist



This is an LTspice schematic drawn for Lab 1 Task 2. The library component MCP6001 uses a model developed by the module lead (Peter Cheung). This model is used as an example for the rest of this lecture.

The op-amp model is a subcircuit, which is indicated by the first character 'X'.

The other components, R, C, V are obvious.

The input and output ports (e.g. V1) are labeled, and their names are used in the LTspice netlist.

For nodes that were not labeled (e.g. V2 source +ve terminal and in- of the op-amp), LTspice generates a label Nxxx automatically, where xxx is a sequence from 001 upwards.

Any line starting with '.' is a SPICE directive – it tells the SPICE simulator what to do instead of specifying the circuit.

The '**.tran 1m**' directive tells LTspice to perform a transient analysis of the circuit lasting for 1msec.

SPICE Cheat Sheet

Letter	Component
R	Resistor
C	Capacitor
L	Inductor
V	independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
X	Subcircuit
E	Voltage-controlled voltage source
G	voltage-controlled current source

Letter	Unit	Multiplier
T, t	tera	10 E+12
G, g	giga	10 E+9
MEG, meg	mega	10 E+6
K, k	kilo	10 E+3
M, m	milli	10 E-3
U, u	micro	10 E-6
N, n	nano	10 E=9
P, p	pico	10 E-12

Directive	Action
.op	DC operating point analysis
.ac	Small signal AC analysis
.tran	Transient analysis
.backanno	Annotate current back to ports
.include	Include another file
.lib	Include a library
.end	End of netlist
.ends	End of subcircuit
.ic	Set initial condition

```
* Netlist for Lab1Task2
R3 VG 0 200k
R2 V1 N002 200k
C1 N001 0 0.1µ
XU1 VG N002 N001 0 V1 MCP6001
V2 N001 0 5
V1 VG 0 SINE(1 0.5 10K)
.tran 1m
.lib /Volumes/External
SSD/Dropbox/_My Documents/MCP6001.mod
.backanno
.end
```

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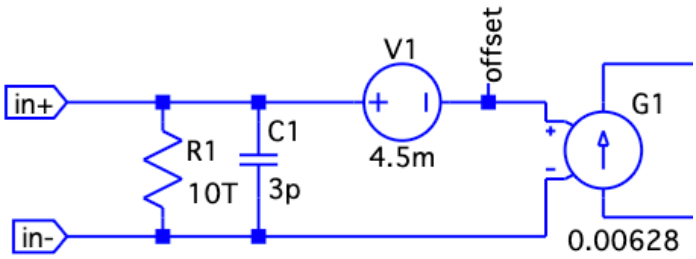
Here are three tables listing:

- common components used in SPICE and LTspice;
- units associated with numerical parameters;
- most used SPICE directives

They are provided here for your reference.

Model input stage of MCP6001

Differential Input Impedance	Z_{DIFF}	—	$10^{13}\|\|3$	—	Ω||pF
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV




```
R1 in+ in- 10T
C1 in+ in- 3p
V1 in+ offset 4.5m
G1 0 int_gain offset in- 0.00628
```

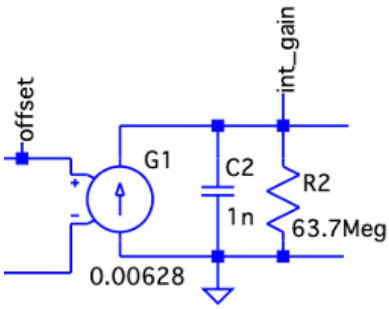

Let us now develop the SPICE model for the MCP6001 op-amp from the datasheet.

Starting with the input stage, the relevant parameters that are modelled here are the differential input impedance (R1 in parallel with C1) and the input offset voltage.

The input impedance is obvious. The input offset voltage models the discrepancy due to input transistor mismatch. Assuming in+ and in- are connected together, there input differential voltage should be 0. However, due to transistor mismatch, the op-amp behaves as if there is an offset voltage of ±4.5mV being applied to the input. This offset voltage is modelled with V1.

The input voltage applied internally is therefore V(offset) – V(in-). This is applied to the gain stage, which is modelled by the voltage-controlled current source G1.

Model gain vs frequency & slew rate of MCP6001




```
...
G1 0 int_gain offset in- 0.00628
R2 int_gain 0 63.7Meg
C2 int_gain 0 1n
```

- Assume compensation capacitor C2 is 1nF

AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1 V/V
Slew Rate	SR	—	0.6	—	V/µs	

DC Open-Loop Gain (Large Signal)	A_{OL}	88	112	—	dB

The next stage of the model consists of G1, C2 and R2.

G1 provide amplification to the differential input voltage and produces an output current to drive R2 at DC. (Remember, at DC, C2 is open circuit.)

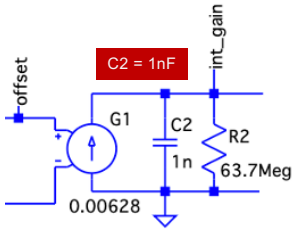
Therefore, the **voltage gain** from input to output of this stage is **G1 x R2**. We want this value to be the DC Open-Loop Gain, which is typically 112dB or 400,000.

We also need to model not just the DC gain behaviour, but the **AC responses**, which include how the gain drops off with signal frequency, how the op-amp changes the phase of the signal, and how fast the output can slew (rise or fall).

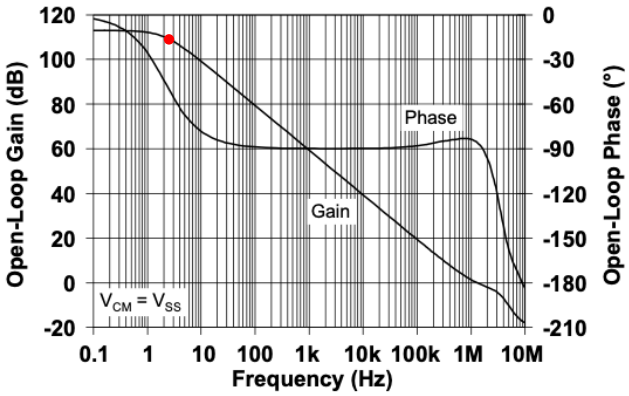
C2 provides part of the modelling. C2 is the internal compensation capacitors which is deliberately inserted into the op-amp to create a 'dominant pole' at low frequency, so that the open-loop gain of the op-amp decreases at -20dB/decade. This is done to ensure that when negative feedback is used, the op-amp remains **stable at all frequencies**.

For our purpose of creating a SPICE model, we assume that **C2**, the compensation capacitor is **1nF.** This is a typical value that is used, but its exact value inside the MCP6001 is NOT important to generate an accurate model. This is because other component values will be chosen based on our choice of C2.

Model open-loop gain vs frequency of MCP6001




```
...
G1 0 int_gain offset in- 0.00628
R2 int_gain 0 63.7Meg
C2 int_gain 0 1n
```



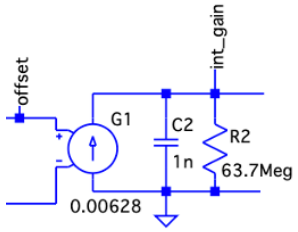
- Dominant pole frequency $f_p = \frac{GBP}{A_{OL}} = \frac{10^6}{400000} = 2.5Hz = 1/2\pi R_2 C_2$.
- Therefore $R_2 = \mathbf{63.7\times10^6\Omega}$
- Calculate gm for G1:

$$gm \times R_2 = A_{OL}, \qquad \text{hence} \quad gm = \frac{400{,}000}{63.7} \times 10^{-6} = \mathbf{0.00628}$$

Consider the Open-Loop Gain and Phase vs frequency plot (Figure 2-11 of datasheet). The DC gain A_{OL} is 112dB. The gain bandwidth product (GBP), the frequency at which the gain drops to 0dB (or 1) is 1MHz. Together, we can calculate that the dominant pole frequency must be $\frac{GBP}{A_{OL}}$. This is because the RC circuit produces a gain drop 20dB (factor of 10) for each decade of frequency increase (also factor of 10). We can therefore extrapolate back from the (0dB, 1MHz) point backwards until it crosses the 112dB line.

at frequencies from 0Hz up to around 2Hz. So the dominant pole created by inserting C2 into the op-amp circuit produces a break frequency (-3dB point) at 2Hz. This frequency is given by $1/2\pi R_2 C_2$.

Model Slew rate limit



AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1 V/V
Slew Rate	SR	—	0.6	—	V/µs	

- Model the slew rate limit of 0.6V/us:

$$SR = max\frac{dV_{c2}}{dt} = \max(current\ of\ G1)\ /C2, \qquad \text{therefore} \quad \max(current) = SR \times C_2 = 0.6mA$$

```
G1 0 int_gain value={limit(0.00628*V(offset,in-),0.6m, -0.6m)}
R2 int_gain 0 63.7Meg
C2 int_gain 0 1n
```

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Next, we need to model the slew rate limit of 0.6V/us.

We know that slew rate is limited by the maximum available charging current to the capacitor C2. Since C2 is 1nF, and SR is 0.6V/us, we can calculate easily that the maximum current should be ±0.6mA from the current source G1.

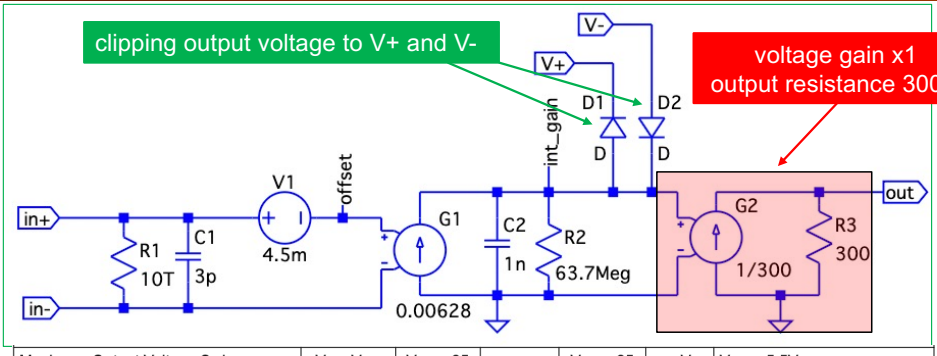
This is specified in the SPICE netlist in the special syntax shown here:

```
value={limit(0.00628*V(offset,in-),0.6m, -0.6m)}
```

This says, G1 output current between terminal 0 and ***int_gain*** is determined as: 0.00628 x controlling voltage between node***_offset*** and node***_in-***. This is further limited to maximum of 0.6mA and minimum of -0.6mA.

This is a powerful feature of SPICE netlist specification. The "**limit**" function provides an easy way to model the slew rate specification.

Model the output stage of MCP6001



Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V, 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V

```
* output stage - current limit to +/- 20mA, ROUT = 300 ohm
G2 0 out value={limit(V(int_gain, 0)/300, 20m, -20m)}
R3 out 0 300
* output voltage limited to V+ and V-
D1 int_gain V+ Dlimit
D2 V- int_gain Dlimit
.model Dlimit D(Ron=0.0001 Roff=100G Vfwd=0)
```


Finally, let us model the output stage. There are two requirements:

1. The output short circuit current should be ±23mA (±20mA used here).
2. The output voltage should not exceed V+ or V-.

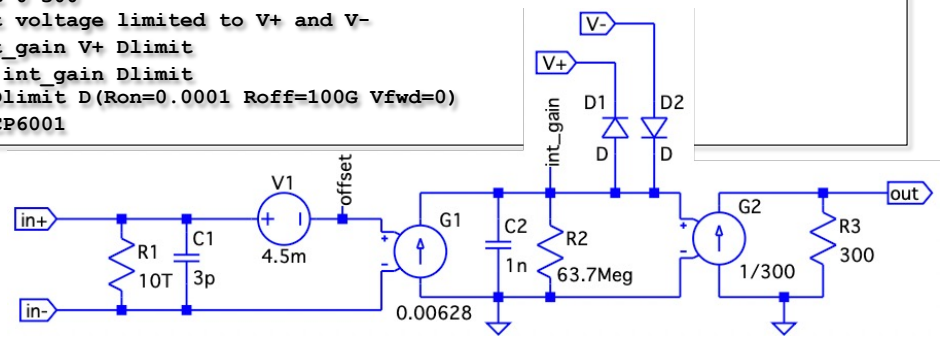
The output stage is modelled with another voltage-controller current source G2 with gm = 1/300. When used with R3=300, the voltage gain is in fact x1. The output impedance of MCP6001 is NOT specified. The 300 ohm is an estimate derived from the manufacturer's SPICE model. However, the current limit of ±20mA is modelled again using the limit function.

The output voltage limit is modelled at the INPUT of G2. Since the voltage gain of the output stage is x1, this provides a convenient way to clip the output voltage without having D1 and D2 interfering with the output load.

Finally, the model used for D1 and D2 has forward voltage set to 0V. That is, the clipping of D1 and D2 is exactly with the power supply value, providing rail-to-rail output. This is not exact because the clipping should occur 25mV earlier. This is not modelled here for simplicity.

The complete model of MCP6001

```
.subckt MCP6001 in+ in- V+ V- out
* input stage - RIN = 10T, CIN = 3p, Voffset = 4.5m
  R1 in+ in- 10T
  C1 in+ in- 3p
  Voffset in+ offset dc 4.5m
* gain stage - R2 = {AOL/(6.28*GBP*CPOLE)}, AOL = 400k, GBP = 1Meg, CPOLE = 1n
* gm = 6.28*GBP*CPOLE, current limit IMAX = +/- 0.6mA
  G1 0 int_gain value={limit(0.00628*V(offset,in-),0.6m, -0.6m)}
  R2 int_gain 0 63.7Meg
  C2 int_gain 0 1n
* output stage - current limit to +/- 20mA, ROUT = 300 ohm
  G2 0 out value={limit(V(int_gain, 0)/300, 20m, -20m)}
  R3 out 0 300
* output voltage limited to V+ and V-
  D1 int_gain V+ Dlimit
  D2 V- int_gain Dlimit
.model Dlimit D(Ron=0.0001 Roff=100G Vfwd=0)
.ends MCP6001
```



Here is a complete model for the MCP6001, including the .subckt statement. To use this model for your design, simply:

1. Download the model as a .txt file from the course webpage by clicking the icon:
2. Save the MCP6001.txt model file in your working folder (for your simulation).
3. Open this file in LTspice.
4. RIGHT-CLICK on the line .subckt and a pop-up window will appear.
5. Select 'Create Symbol'.
6. Under file, select 'Save as', and save this new op-amp symbol in the 'Autogenerated' folder.

Thereafter, MCP6001 will appear as a component in your library, and the symbol is linked to the MCP6001.txt model file.

For MCP6002, just instantiate MCP6001 twice.

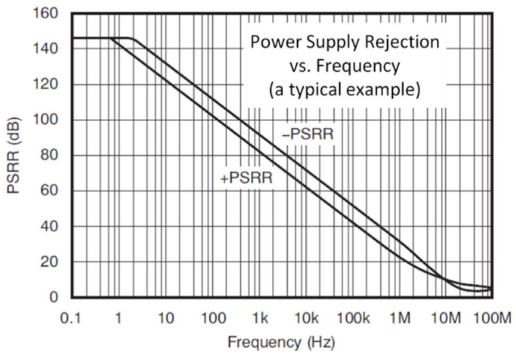
What specifications are NOT modelled?

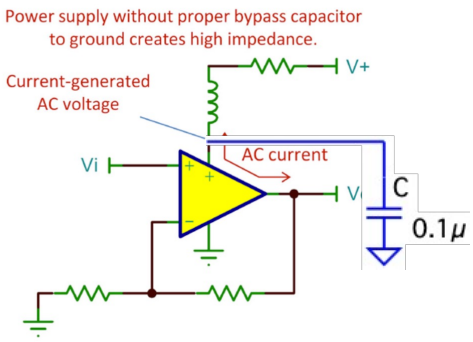
- Common mode input impedances
- Common mode rejection ratio
- Power supply rejection ratio
- Common mode input voltage clipping
- Temperature effect on input bias current and offset voltage
- Noise characteristics of the op-amp
- Quiescent current of the op-amp

The MCP6001 model is deliberately simplified to exclude the specifications above. The reasons for doing so are:

1. The simplified model results in much faster simulation.
2. None of these omitted specification impact the lab experiments.
3. These are generally secondary specifications and therefore the impact is also secondary.
4. Finally, it allows the development of the model in this lecture easier to understand.

Power supply bypass (decoupling) capacitor





- Wire connection from power supply to op-amp power pin is an inductor.
- Inductor has high impedance at high frequency.
- Current draw through op-amp causes current fluctuation in inductor – can feedback to the op-amp.
- Resulting in op-amp prone to oscillation at high frequency or output overshoot.
- Add ceramic or tantalum capacitor close to op-amp supply pin to bypass (or decouple) any such high frequency fluctuations.

Lab 1 op-amp circuits all include a 0.1uF capacitor from the power supply pin to ground. This is known as decoupling or bypass capacitor. Why is it necessary?

All supply connections using wire are inductors at high frequencies. This can pick up ambient noise signals to the supply of the op-amp. Shown here is the op-amp's power supply rejection ability, which deteriorates at high frequency. A bypass capacitor will short out such noise to ground.

Further, as the op-amp (or any other type of electronic circuits) amplifies a signal and drives a load, varying current is drawn from the power supply pin. With the inductance of the connecting wire, this signal could find its way back to the op-amp input through some unintended path, and there is a risk of providing a positive feedback path, resulting in oscillation.

The bypass/decoupling capacitor solves the problem by providing a low impedance path to ground at high frequencies.